An Automated Control Code Generation Approach for the SegBus Platform

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***Abstract*—We present here a model-driven approach for the generation of low-level control code for the arbiters, to support application implementation and scheduled execution on a multi-core segmented bus platform, SegBus. The approach considers Model-Driven Architecture as a key to model the application at two different abstraction levels, namely as Packet-Synchronous Dataflow and Platform Specific Model, using the SegBus platform's Domain Specific Language. Both models are transformed into Extensible Markup Language schemes, and then utilized by an emulator program to generate the "application-dependent" VHDL code, the so-called "snippets". The obtained code is inserted in a specific section of the platform arbiters. We present an example of a simplified stereo MP3 decoder where the methodology is employed to generate the control code of arbiters.**

I. Introduction

The decreasing technological figures cause modern day designers to move towards on-chip multiprocessing technologies. New architectures are brought into context in order to utilize the tremendous advances of fabrication technology. Distributed on-chip architectures or multiprocessor system-on-chip (MPSoC) paradigm gains increasing support from system designers. MPSoC is seen as one of the foremost means through which performance gain are still to be sustained even after Moore's law may become decrepit [1].

As the complexity of the application requirements is increasing with time, the designers are facing difficulty while designing applications targeting MPSoC. However, it has also been a challenge to fully benefit from the features of MPSoC platforms. The current design methodologies don't provide full automation in every level of the development process, and sometimes, the communication characteristics of the platforms and the employed devices also do not match. In order to offer an optimum match, platform specific characteristics must be taken into consideration for each application.

The approach we deliver in this paper is based on establishing a design methodology for MPSoC, in the context of the *SegBus* platform [2]. In our previous work [5][6], we have already introduced a *Domain Specific Language* (DSL) and an *emulator* program for modeling and emulating applications at *Platform Specific Model* (PSM)-levels. We deliver here methods to update the DSL and emulator to make them capable for the modeling of application at *Packet-Synchronous Data Flow* (PSDF)-level, and introduction of automated methods within emulator program to generate transaction-level control code in the form of VHDL *snippets*, in order to successfully implement a given application on the distributed platform at hand. We introduce procedures to transform PSDF and PSM models into XML schemas with the help of modeling tool [7]. The generated XML of the PSDF and PSM models are then used by the *emulator* [6] program to assess the performance aspects. If we find the performance aspects up to an optimum level, the current research work addresses issues how we generate the transaction-level control code from the emulator program in an automated way.

The generation of control code and their realization is especially necessary as the platform doesn't require (or benefit) from an operating system solution. Seceleanu et. al. [8] provided definition of the *SegBus*'s arbiters' control structures. The definition comes in the form of (manually obtained) VHDL code snippets that provide the transfer schedule, such that arbiters organize the execution following the application specification. In this paper, we continue our efforts towards an automated design framework.

Related Work. In recent years, MDA has been utilized in different design areas to provide automation up to some extent.

Vidmantas et al. [9] introduced MDA methods where the designer can model application as PIM model using UML together with SysML plugin. They introduced techniques to transform PIM into PSM model, which is later transformed into source code specifically for one operating system (OS). The authors have considered more than one OS where the modeled application can be run, unlike our case where there is no consideration of OS is required.

Koudri et al. [10] presented design flow for System-on-Chip/System-on-Programmable Chip design, based on the use of UML and dedicated profiles. They supported the use of the Model-Driven Development for the hardware-software co-design with an example of *Cognitive Radio Application*, implemented on FPGA. The modeling tool they used generated thousands of lines of code for the modeled example application but further improvements needs to be done, particularly in the Model of Computations support.

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II. Background

A. Segmented Bus Architecture

A segmented bus is a "collection" of individual buses (segments), interconnected with the use of FIFO like structures. Each segment acts as a normal bus between modules that are connected to it and operates in parallel with other segments. Neighboring segments can be dynamically connected to each other to establish a connection between modules located in different segments. Due to the segmentation of the bus lines, and their relative isolation, parallel transactions can take place, thus increasing the performance. A high level block diagram of the segmented bus system which we consider in the following sections is illustrated in Fig. 1.

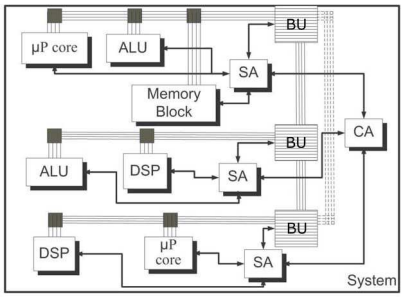

Fig. 1. Segmented bus structure.

The *SegBus* communication platform is built of components that provide the necessary separation of segments - *Border units* (***BU***), arbitration units - the *Central Arbiter* (***CA***) and local, *Segment Arbiters* (***SA***). The application then is realized with the support of (library available) *Functional Units* (***FU***).

The *SegBus* platform has a single ***CA*** unit and several ***SA***s, one for each segment. The ***SA*** of each bus segment decides which device (***FU***), within the segment, will get access to the bus in the following transfer burst.

Platform communication. Within a segment, data transfers follow a "traditional" package based bus protocol, with ***SA***s arbitrating the access to local resources. The inter-segment communication, is also a package based, circuit switched approach, with the ***CA*** having the central role. The interface components between adjacent segments, the ***BU***s, are basically FIFO elements with some additional logic, controlled by the ***CA*** and the neighboring ***SA***s.

B. DSL for the SegBus Platform

The *Domain Specific Language* (DSL) for the *SegBus* platform is the specification language that is used to model the *SegBus* platform at higher-level of abstraction, based on stereotypes stored in the *SegBus* UML profile [5]. The DSL provides ability to model platform elements in the form of high-level graphical constructs and provide methods to map partitioned application components on particular segment in a fast and correct manner.

The DSL comprises of a number of structural constraints related to the platform, written in *Object Constraint Language* (OCL) [11], to implement the correct component approach to platform design. These constraints are used to validate our models. Upon breach of any constraint requirement during the design process, the tool provides appropriate error message, so that the designer can take proper action to make the model correct according to platform requirements.

Before the current work, the DSL was only capable of modeling application at PSM-level. Here, we add capabilities to model application at PSDF level, too. We introduce three new stereotypes, that is, *InitialNode*, *ProcessNode* and *FinalNode*, in the UML profile of DSL. The profile defines the main structural elements of the platform. The new stereotyped classes related to PSDF are generalization of the metaclass *UML Standard Profile::UML2MetaModel::Classes::Kernel::Class*. We also introduced their related customization classes and set tags with suitable values. We skip here further details about tag values intentionally because of the space limitation.

Once we model the application components as PSDF, model the platform and map the application components on to the platform correctly, we apply validation process to get the correct *Platform Specific Model* (PSM) of the application. If there exists some errors in the model, we get error message(s) and associated model element become highlighted.

Finally, the PSDF and PSM model can be transformed into XML schema for further analysis of the desired platform configuration. We employ the generated XML schemas for emulating the performance aspects of the configured system, as described in the next section.

C. SegBus Emulator

The *SegBus Emulator* enables us to evaluate the performance aspects of any given application running on a specific platform configuration, defined during modeling [6]. The emulator supports the analysis of various *SegBus* instances that may answer, better or worse, to specific application requirements. It helps to decide at early stages of design process which platform configuration will be most suitable for any given application before moving towards lower abstraction levels. The code generation engine, supplied by the *MagicDraw UML* [7] tool transforms PSDF and PSM of the system into XML schemas. The generated XML schemas are then employed by the emulator program to estimate the utilization of platform elements with respect to data transfers and total execution time. After the analysis of the returned results, the designer is able to make decision at this stage whether the emulated configuration will be best/optimal or not, for the target application, and can change it before moving towards lower levels of the design process. After getting the desired platform configuration for a given application, the next step is to generate the execution schedule in the form of VHDL snippets, to be later used by the arbiters.

III. Design Methodology

We employ the *MagicDraw UML* tool for graphically modeling the application at PSDF and PSM level, and transforming it into XML schemas. Fig. 3 illustrates the design methodology

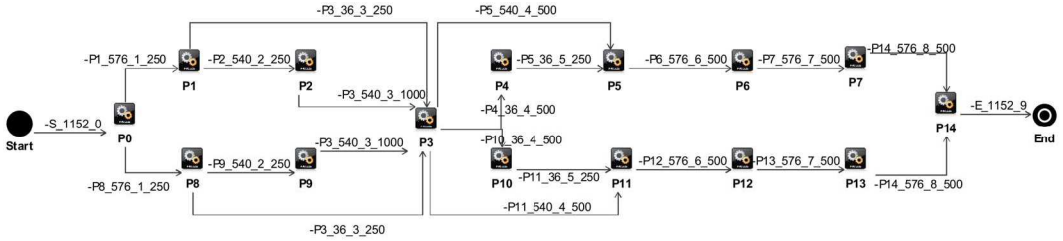

Fig. 2. PSDF model of the example application employing DSL.

employing DSL and emulator. We demonstrate our approach with the help of a (simplified) stereo MP3 decoder [12] application.

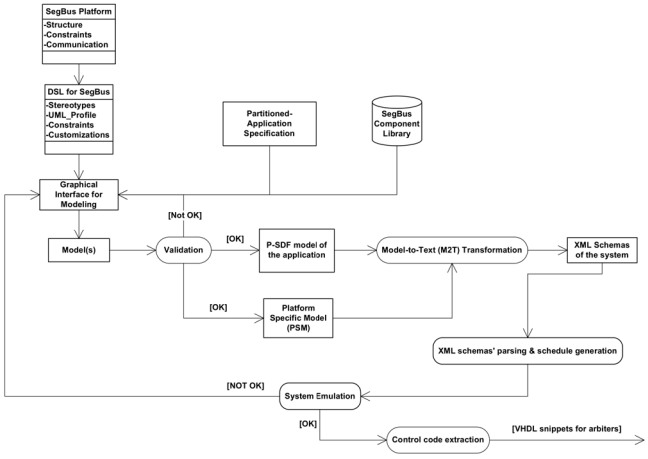

Fig. 3. Design process of the SegBus platform using DSL and emulation.

A. The Packet SDF

The specification of the application itself starts with a *Packet SDF* (PSDF) model. PSDF is a customized version of Synchronous Data Flow diagrams [13]. The approach is intended to facilitate the mapping of the application to the architecture due to the similarity between the operational semantics of the PSDF and that of the *SegBus* architecture, thus allowing us to cope in a more detailed manner with the communication characteristics of our platform.

A PSDF comprises mainly two elements: *processes* and *data flows*; data is organized in packets according to package size during execution. Processes transform input data packets into output ones, whereas packet flows carry data from one process to another. A *transaction* represents the sending of one data packet by one source process to another, target process, or towards the system output. A *packet flow* is a tuple of four values, P_t, D, T and C. The P_t value represents the target process for the given transactions; the D value represents the number of data items emitted by the same source, towards the same destination; the T value is a relative ordering number among the (package) flows in one given system; and the C value represents the number of clock ticks a process consumed before sending one package. Thus, a flow is understood as the number of data items (later transformed into packets) issued by the same process, targeting the same destination, having the same ordering number and same clock ticks require to process one individual package.

If s is the package size (number of data items in a package) in the platform configuration, then the *Packet SDF (PSDF)* of a certain system is a sequence of packet flows, $< (P_{t_x}, \frac{D_1}{s}, T_1, C_1), \ldots, (P_{t_x}, \frac{D_n}{s}, T_n, C_n) >$, where $\forall i, j, x \in \{1, \ldots, n\} \cdot \frac{D_i}{s} \neq \frac{D_j}{s}$ and $T_1 \leq T_2 \leq \ldots \leq T_n$.

The non-strictness of the relation between T values of the above definition models the possibility of several flows to coexist at moments in the execution of the system.

B. Application Modeling

The specification starts with the context diagram of the application, where the interactions between the application (depicted as a process) and the external environment are modeled in terms of input/output data-flows. In subsequent steps, the top-level process is decomposed hierarchically into less complex processes and the corresponding data-flows between these processes.

The decomposition process is based on designer's experience and ends when the granularity level of the identified processes maps to existent *SegBus* library elements or devices that can be developed by the design team. We employed *SegBus* DSL to represent the PSDF. The PSDF model of the example application is given in Fig. 2, where process *P0* represents frame decoding, *P1/P8* - scaling on the left/right channel, *P2/P9* - dequantizing left/right channel, etc.

The PSDF model serves as the *Platform Independent Model* (PIM) of the application. We consider further a *three* segments platform configuration and map the application processes using the design methods described in [5]. Fig. 4 depicts the PSM model of the example application. Later on, we transform the PSDF and PSM models of the application into XML schemas using M2T transformation supplied by the tool. The XML schema contains information about platform elements, application processes in the form of ***FU*** and their relative placement on different segments. The XML consists of a *schema* element and a number of sub-elements, in the form of *complexType* and *element* types.

Each complex type represents a platform element (***CA***, ***SA***, etc.) or application component (P0, P1, etc.). The *name* attribute of each complex type shows the name of the element. Furthermore, each complex type may contain sub-elements.

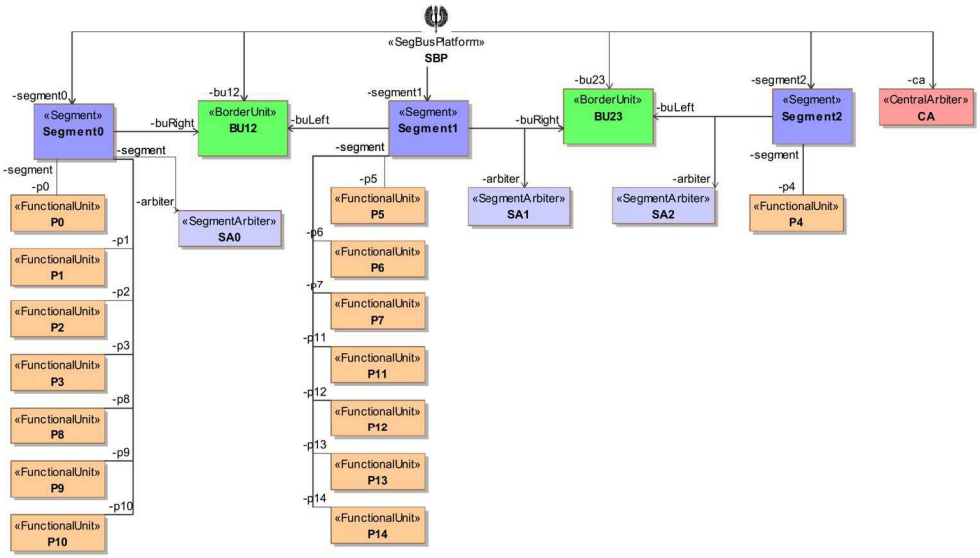

Fig. 4. PSM model of the example application in 3 segments, linear topology configuration.

Following, we show an XML snippet of the PSDF model after transformation, consisting of process *P0*, *P1* and their relative transfers to other processes.

```
<xs:complexType name="P0">
     <xs:sequence>
         <xs:element name="P1_576_1_250" type="P1"/>
       <xs:element name="P8_576_1_250" type="P8"/>
   </xs:sequence>
</xs:complexType>

<xs:complexType name="P1">
     <xs:sequence>
         <xs:element name="P2_540_2_250" type="P2"/>
       <xs:element name="P3_36_3_250" type="P3"/>
   </xs:sequence>
</xs:complexType>
```

Below is the piece of XML snippet of PSM model after transformation, representing the *SegBus* platform instance (*SBP* with three segments as child-elements) and "*Segment 1*" element with its child-elements.

```
<xs:complexType name="SBP">
   <xs:all>
      <xs:element name="segment0" type="Segment0"/>
      <xs:element name="segment1" type="Segment1"/>
      <xs:element name="segment2" type="Segment2"/>
      <xs:element name="ca" type="CA"/>
      <xs:element name="bu12" type="BU12"/>
      <xs:element name="bu23" type="BU23"/>
   </xs:all>
</xs:complexType>

<xs:complexType name="Segment1">
   <xs:all>
      <xs:element name="buRight" type="BU23"/>
      <xs:element name="buLeft" type="BU12"/>
      <xs:element name="p5" type="P5"/>
      ...
      <xs:element name="p14" type="P14"/>
      <xs:element name="arbiter" type="SA1"/>
   </xs:all>
</xs:complexType>
```

The *communication matrix* is the specification of device-to-device transactions between application components. Each entity in the communication matrix describe how many data items need to be transfered from one device to any other device. The emulator program builds the matrix by extracting transactions between processes in PSDF model. Based on the matrix, the *PlaceTool* application [14] finds the optimal device allocation solution, given the platform specifics (the number of segments).

The emulation and control code generation processes are based on both PSDF and PSM. The PSDF model provides information about interaction between application processes with required data items and other useful parameters, while the PSM model represents the placement of each application process on different segments of the platform. Hence, the emulator program parses XML of both models to be later used for emulation and control code generation. During the parsing process, the emulator extracts following information from the PSDF model:

- Number of application processes.
- Data transfers from each process.
- Ordering of transfers.
- Clock ticks to be consumed by each process while processing one package.

The emulator stores above information in temporary variables and arrays inside the program. For instance, the name attribute from one of the *element* from *P0*, that is, "P1 576 1 250" represents a transfer from process *P0*. The " " character serves as the separator between the entities. The first entity "*P1*" represents the target process of this transfer; the second entity "576" is the number of data items to be transferred; the third entity "1" is the sequencing order and the last entity "250" is the number of clock ticks a process needs to consumed before sending each package.

Furthermore, the emulator extracts following information from the PSM model and stores in a number of variables and arrays inside the emulator, too:

- Number of segments in the platform.
- Number of border units based on platform geometry.
- Placement of application processes on different segments.
- ..

When the parsing process is finished, the emulator iterates in the previously populated arrays, instantiates the required ***FU***s and pass them necessary information. This necessary information contains number of data items to be transferred, destination processes, relative ordering, clock ticks a process needs to be consumed before sending a package and placement in the specific segment.

The *contructor* method of the ***FU*** class analyzes the passed information to it and instantiates the required number of objects of *masters* and *slaves*, which later run as threads during emulation. Finally, the values in the temporary variables and arrays within the emulator application are later used for extracting the control code of the arbiters. As per emulator functionalities, we can generate the control code from the supplied XML schemas without performing the emulation, but it is always recommeded to emulate the modeled platform configuration before moving towards the later stages of the design process.

Without considering details, the control flow of both ***SA***s and of the ***CA*** is represented in Fig. 5.

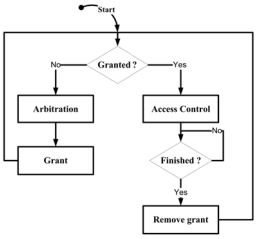

Fig. 5. Arbiter control flow.

The ***SA***s and the ***CA*** are VHDL defined modules, with a similar structure. The code implements the operational flow of Fig. 5, running with multiple parameters as required by the platform specification. We see the application as a set of correlated transactions that must be ordered in their execution by the arbiters. The specification of the schedule - as supplied by the PSDF representation, is provided by a snippet introduced in the ***SA*** or the ***CA*** codes, representing the projection of the application flow at the respective level and location. The snippets correspond to the middle block - "Arbitration specification" in the arbiter structure of Fig. 6.

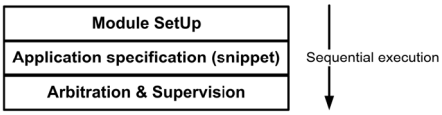

Fig. 6. Arbiter code structure.

The emulator program reads the package size, PSDF and PSM models in the form of XML schemas and runs the emulation. Upon completion, the tool returns results of the transactions from each platform element, performed during execution. At this stage, it's the job of the designer to evaluate the emulation results and modify the design, if needed. Later on, we generate the transaction-level control code (in the form of synthesizable VHDL snippets) of the arbiters to be used in the final implementation. Following, we show an excerpt from the generated control code for the example application.

```
--    VHDL Snippet for "Segment 0"
program(0) <= (guard => 0, source => 0, dest => 1,
   dest_seg => 0, togrant => 0, count=16, enables=13);
program(1) <= (guard => 0, source => 1, dest => 8,
   dest_seg => 0, togrant => 1, count=16, enables=2);
program(2) <= (guard => 1, source => 2, dest => 2,
   dest_seg => 0, togrant => 2, count=15, enables=3);
...
program(12) <= (guard => 1, source => 8, dest => 11,
   dest_seg => 1, togrant => ToR, count=1, enables=0);
```

Each line in the above control code is an *execution line* of the respective arbiter. The *program* is a multi-dimentional vector consisting of a number of execution lines with several further fields. Below is a brief discription of each field of the execution line.

• *program(x).* Basically, x can be seen as the *Program Counter*, and *program(x)* represents the x line of arbitration code.

• *guard.* When *guard* = 0, the respective line is *enabled*, that is, the arbiter may consider it for selection. When *guard* $>$ 0, the line is disabled, that is, it cannot be considered in the arbitration. The arbiter marks a line as *executed* whenever the respective *count* value reaches 0, by establishing *guard* = *nrLines*, since *nrLines* is the total number of program lines in the *program* vector, associated with the given arbiter.

• *source.* For ***SA*** case, this field contains the address of the requesting master - the initiator of a transfer request. Devices on the *SegBus* platform (masters, slaves) are identified by an unique number. For the ***CA***, this field contains the address of the initiating *segment*.

• *dest.* The address of the targeted device - the slave.

• *dest seg.* The target slave's segment address.

• *toGrant*. This is the instruction for the arbiter to grant the requesting master. At this moment the field is preserved for future developments.

• *count*. This field identifies the number of packages the master has to send to the specified slave.

• *enables*. Whenever a line is marked *executed*, the ***SA*** will *enable* the execution line specified by this field, by subtracting 1 from its current *guard* value. If, for a given line, *enables* = *nrLines*, then the arbiter does not try to enable any other line, when the current one is marked *executed*.

In addition, we use the notations: ToR/ToL - the destination is the ***BU***to the right / left of the current ***SA***); RFL - the request comes from left.

When the parsing process is done, the emulator creates:

• The *accCAArray*: a single-dimensional array, where each element in the array represents an execution line of the ***CA***.

• The *accArray*: a 2-dimensional array where each column represents an execution line of a ***SA***, while each row consists

of execution lines associated with any particular ***SA***.

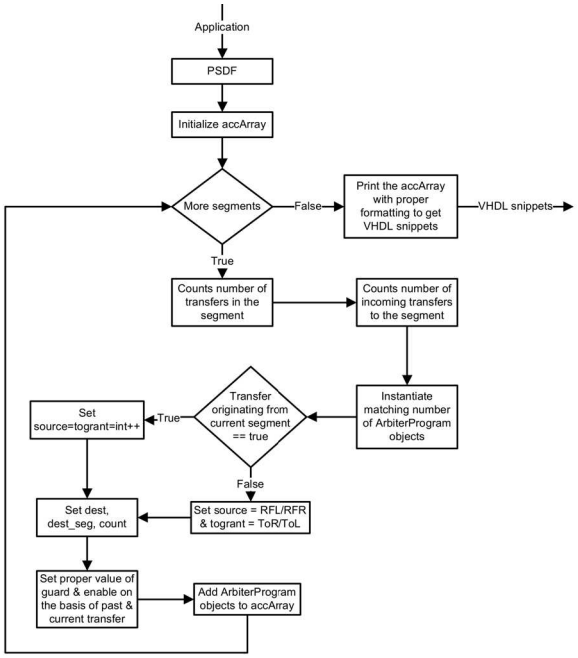

Fig. 7. Code extraction process for segments in the platform.

Fig. 7 illustrates the general flow of the code generation process for segments after the parsing of the PSDF model has been done and the model resides now inside the emulator's internal variables and arrays. Firstly, the emulator analyzes number of originating and incoming transfers in each segment. On the basis of this information, it creates equal number of *ArbiterProgram* objects. Secondly, it sets the *dest* field with the target process ID and *dest seg* field with the segment ID where the target process is placed. If the transfer is originated from a master in the current segment, then it sets the *source* value of each object with an integer number in increasing order and *togrant* = *source*, otherwise the transfer is considered to be coming from a different segment via left/right ***BU***. In this case, the *togrant* = *ToR/ToL* and *source* = *RFL/RFR* are set according to the direction of the transfer. The *count* contains number of packages for this transfer (data items divided by the package size). The *program* field contains the order number of the execution line and the *sequence* field contains the relative order number of the execution line according to PSDF model.

The *guard* and *enables* fields are important to introduce parallelism in the platform. An execution line is executed by the respective ***SA***, when its *guard* signal is zero. The emulator application sets the values of *guard* and *enables* field on the basis of ordering sequence of transfers. If two or more transfers occur at the same ordering sequence, it sets appropriate values to both fields so that parallel transfer can occur. For instance, the PSDF model of the example application in Fig. 2 contains two parallel transfers from process *P0* at sequence order 1. As per application requirements, both transfers needs to be completed in parallel before moving towards further transfers. The execution lines associated with these two transfers are given below:

```
program(0) <= (guard => 0, source => 0, dest => 1,
   dest_seg => 0, togrant => 0, count=16, enables=13);
program(1) <= (guard => 0, source => 1, dest => 8,
   dest_seg => 0, togrant => 1, count=16, enables=2);
```

A similar approach is taken with respect to the VHDL code to be generated for the ***CA*** operations.

IV. Conclusions

We have introduced MDA-based design methods to generate the transaction-level control code for a distributed platform, the *SegBus*. We have described methods to model application at PSDF and PSM levels by employing *SegBus DSL* and run emulation using *emulator* program to get performance aspects of the modeled configuration. The emulator program has further modified to generate the arbiters' low-level control code, in the form of VHDL *snippets*, which are then to be inserted in a specific block of (segment or central-level) arbiters as an execution schedule for any given application.

Acknowledgments

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